WHAT IS CLAIMED IS:

1. A virtual computer verification platform, comprising:

a simulation system which includes a special function for integrating a microprocessor chip with the simulation system, a concurrent-clock circuit inserted into said microprocessor chip, a peripheral chip simulation subsystem, a peripheral device simulation subsystem and a bus command compiler; and

a set of on-line debugging auxiliary tools which are connected to said virtual computer simulation system for modifying the contents of said peripheral device to assist said microprocessor chip in debugging.

2. The virtual computer verification platform according to claim 1, wherein said microprocessor chip is designed in a Behavior model, a RTL model and a Gate model.

3. The virtual computer verification platform according to claim 1, wherein said microprocessor chip is coded in a high level hardware description language, Verilog.

4. The virtual computer verification platform according to claim 1, wherein said special function is vpm_call ( ) written in a C high level programming language and is used for transferring an interface signal from said microprocessor chip to said peripheral chip simulation subsystem through a message passing mechanism supported by UNIX IPC (Inter-Process Communication) and PLI (Programming Language Interface) supported by Verilog.

5. The virtual computer verification platform according to claim 4, wherein said concurrent-clock circuit is used for creating a synchronic clock between said simulation system and said microprocessor chip, collecting said interface signal from said microprocessor in each clock

cycle, delivering said special function into said simulation system beyond said microprocessor chip in a leading edge and a trailing edge of each synchronic clock cycle, and waiting for a result to achieve synchronic transfer and data transfer.

6. The virtual computer verification platform according to claim 1, wherein said peripheral chip simulation subsystem is used for integrating each individual virtual peripheral chip and is designed in terms of an object-oriented programming technology for providing a peripheral control chipset of the simulation system with performance, interface protocol and clock.

7. The virtual computer verification platform according to claim 1, wherein said peripheral device simulation subsystem is used for integrating individual virtual peripheral device and is designed in terms of an object-oriented programming technology for providing a peripheral device of the simulation system with performance.

8. The virtual computer verification platform according to claim 1, wherein said bus command compiler is used for compiling a protocol signal command from said microprocessor chip and transferring a compiled command into said peripheral chip simulation subsystem.

9. The virtual computer verification platform according to claim 1, wherein said set of on-line debugging auxiliary tools comprises:

a Graphic User Interface which is implemented by using a C++ programming language in terms of a X-Windows, a Motif program library, a UNIX standard system service program library, a Perl programming language and a Tcl/Tk;

a first compiler for displaying and revising contents of a memory;

a second compiler for displaying and revising contents of a virtual

harddisk;

a set of harddisk low level management tools capable of reading a parameter table of the virtual harddisk and formatting the virtual harddisk in low level;

a set of MS-DOS compatible file system management tools for implementing a file system operation of simulation system when no operating system is executed, including partition and labeling of the harddisk, formatting a MS-DOS file, copying a file, deleting a file, establishing a directory, and deleting a directory for facilitating the operation system installation of the simulation system; and

a Basic Input Output System (BIOS) chip written tool for writing a ROM image file of a new BIOS program into said microprocessor chip of said simulation system.